



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,225	12/15/2000	Chien-Ping Huang	EM/HUANG/6315	8653

7590 02/15/2002  
BACON & THOMAS  
625 Slaters Lane - 4th Floor  
Alexandria, VA 22314

EXAMINER

PAREKH, NITIN

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 02/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/736,225

Applicant(s)

Huang et al

Examiner

Nitin Parekh

Art Unit

2811



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jan 3, 2002
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirements.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_

Art Unit: 2811

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawahara et al (US Pat. 6111306).

Regarding claims 1 and 3, Kawahara et al disclose a semiconductor package comprising:

- an interim substrate having front and back surfaces
- an insulating material (559 in Fig. 135A) comprising conventional polyimide/solder mask (507 in Fig. 126C and 135A-F; Col. 59, line 30) formed at selected locations on the front surface of the interim substrate
- a lead layer and a die pad layer (508 and 504 in Fig. 126C respectively) formed on the front surface of the interim substrate not covered by the insulating material/solder mask
- a chip (501 in Fig. 126C) adhering to the die pad layer

Art Unit: 2811

- a plurality of conductive elements/wires (513 in Fig. 126C) electrically connecting the chip and lead layer, wherein
  - the interim substrate is removed/etched (Fig. 135E/F; Col. 72, line 5-50) on a singulated/separated package, and
  - a molded resin (503 in Fig. 126C) covering the chip, conductive elements/wires, polyimide/solder mask, lead layer and die pad layer.
- (Fig. 126C, 135A-F; Col. 62, line 42- Col. 63, line 30; Col. 67, line 13-66).

Kawahara et al fail to specify the process sequence/steps in the order of singulating/separating the packages followed by etching the interim substrate.

Applicant's claim 1 do not distinguish over Kawahara et al regardless of the process for the etching/removing the interim substrate and singulating the packages, because only the final product is relevant, not the process of making such as "etching followed by singulating or singulating followed by etching". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a

Art Unit: 2811

new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Therefore, it would be obvious to a person of ordinary skill in the art at the time invention was made to incorporate etching of the interim substrate after the package is singulated to reduce the dicing defects and manufacturing yield in Kawahara et al’s package.

Regarding claim 7, Kawahara et al fail to specify using the conductive elements/wires being made of a material selected from the group consisting of gold, copper or aluminum.

It is conventional in the chip packaging art to use the conductive elements/bonding wires made of a material such as gold, copper, aluminum, etc (see IDS reference, paper #2: Takebe, Col. 3, line 61).

Therefore, it would be obvious to a person of ordinary skill in the art at the time invention was made to use the conductive elements made of a material selected from the group consisting of gold, copper or aluminum to achieve the desired resistance in Kawahara et al’s package.

Art Unit: 2811

3. Claims 2, 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawahara et al (US Pat. 6111306) in view of Fukutomi et al (US Pat. 5976912) and Fjelstad et al (US Pat. 6001671).

Regarding claims 2 and 8, Kawahara et al disclose the interim substrate and die pad being made of an organic material and copper respectively (Col. 59, line 36; Col. 71, line 65) but fail to specify those being made of copper and solder mask.

Fukutomi et al teach using conventional substrate material such as copper and polyimide resin/solder mask (1 and 16 respectively in Fig. 8a-e; Col. 12, line 15-45; Col. 11, line 35) for the interim substrate and die pad respectively.

Therefore, it would be obvious to a person of ordinary skill in the art at the time invention was made to incorporate the interim substrate and die pad being made of copper and solder mask to reduce process defects and improve die support structure using Fukutomi et al's substrates in Kawahara et al's package.

Regarding claims 4 and 6, Kawahara et al disclose the lead layer and die pad layer being made of conductive copper (Col. 65, line 35; 508/504 in Fig. 126C) but fail to specify those being made of conductive material consisting of nickel and gold formed by plating.

Fukutomi et al teach using conventional plating of nickel and gold in forming the conductive layers (2 in Fig. 8a-e; Col. 12, line 20).

Art Unit: 2811

Therefore, it would be obvious to a person of ordinary skill in the art at the time invention was made to incorporate the material consisting of nickel and gold in forming the lead layer and die pad layer using a plating process to improve the adhesion and wire bonding using Fukutomi et al's wiring design in Kawahara et al's package.

Regarding claim 5, Kawahara et al disclose the polyimide/solder mask being formed by performing punching process (Fig. 135A/125B; Col. 65, line 29) at selected locations on the front surface of the interim substrate but fail to specify using a photolithography process.

Fukutomi et al teach using screen printing process in forming the polyimide/solder mask pattern (Fig. 8b; Col. 12, line 27). Fukutomi et al further teach using conventional processes such as photolithography for exposing/printing of photosensitive polyimide (Col. 11, line 35).

Therefore, it would be obvious to a person of ordinary skill in the art at the time invention was made to perform photolithography on polyimide/UV-curable resin to improve the dimensional accuracy and control for the wiring/leads using Fukutomi et al's wiring design in Kawahara et al's package.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

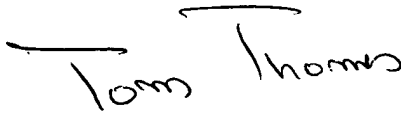
Art Unit: 2811

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

02-07-02

  
**TOM THOMAS**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**